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SOLAR ENERGY CONVERSION SYSTEM USING SIMPLIFIED MULTI LEVEL INVERTER

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ABSTRACT

Multilevel converters offer high power capability, associated with lower output harmonics and lower commutation losses. their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. this work reports a new multilevel inverter topology using an h-bridge output stage with a bidirectional auxiliary switch. the new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output. the new topology is used in the design of a five-level inverter; only five controlled switches, eight diodes, and two capacitors are required to implement the five-level inverter using the proposed topology. the new topology achieves a 37.5% reduction in the number of main power switches required (five in the new against eight in any of the other three configurations) and uses no more diodes or capacitors that the second best topology in the literature, the asymmetric cascade configuration. additionally, the dedicated modulator circuit required for multilevel inverter operation is implemented using a fpga circuit, reducing overall system cost and complexity. theoretical predictions are validated using simulation in spice, and satisfactory circuit operation is proved with experimental tests performed on a laboratory prototype.

index terms—capacitor clamped, diode clamped, field programmable gate array (fpga), h-bridge, multilevel inverter.

I. INTRODUCTION

THE different topologies presented in the literature as multilevel converters [1] show a number of characteristics in common, giving them some clear advantages over bilevel onverters, such as:

—reduction in the commutation frequency applied to the power components; —reduction in the voltages applied to the main power switches, enabling operation t higher load voltages; — transient voltages automatically limited.

The main disadvantage associated with the multilevel configurations is their circuit complexity, requiring a high number of power switches that must be commutated in a precisely determined sequence by a dedicated (and complex) modulator circuit; they also require a great number of auxiliary dc levels, provided either by independent supplies or, more commonly, by a cumbersome array of capacitive voltage dividers. In this case, ensuring that the dc voltages are kept in equilibrium is another factor that increases the complexity of the modulator circuit. In the past, these disadvantages were almost overwhelming,

due to the cost differences they produced between multilevel and standard configurations. Multilevel converters were used only in some high power applications such as high power motor drivers in marine, mining, or chemical industries applications, high power transmission, power line conditioners, etc. [2].

In all these applications their advantages compensate the cost differential. The continuing development of high power high switch frequency devices such as insulated-gate bipolar transistors (IGBTs) working at 3.3, 4.5, and 6.5 kV, and insulated-gate commutated thyristors (IGCT) working at 4.5 or 6 kV has improved overall converter performance, enewing the interest in multilevel topologies, that may be able to compete in the market with the standard two-level pulsewidth modulation (PWM) converters at lower power ranges. Initially, the main interest was concentrated in three-level configurations but recently four- and five-level converters have also been reported. Even taking into account the technological tendency to lower the prize at which multilevel converters can compete with standard configurations, the prize difference will remain unless the complexity issue is solved both at the power circuit and at the modulator circuit levels. As a contribution to solve

These twin problems (cumbersome power stages and complex firing control circuits), this work roposes a new converter topology, presented as a block diagram in Fig. 1. This topology includes an H-bridge stage with an auxiliary bidirectional switch, drastically reducing the power circuit complexity, and a modulator and firing control circuit developed using a field programmable gate array (FPGA) programmable circuit, to simplify the modulator circuit design and implementation. These two concepts are used in the design of thefive-level bridge converter presented below. The new converter topology used in the power stage offers an important improvement in terms of lower component count and reduced layout complexity when compared with the five-level converters presented in the literature. The new topology achieves almost a 40% reduction in the number of main power switche required and uses no more diodes or capacitors that the second best topology, the asymmetric cascade configuration [1]. In the modulator circuit, the FPGA can perform all required modulation functions, providing another important reduction in cost and circuit complexity.

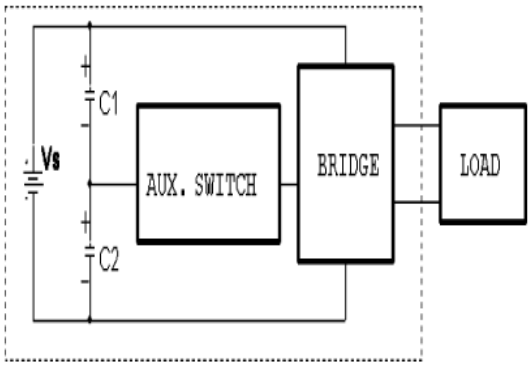


Fig. 1. New topology block diagram.

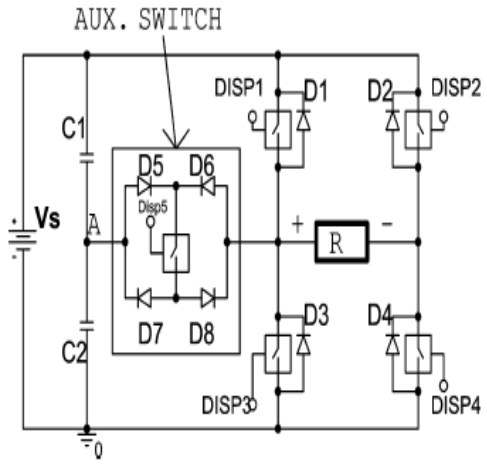


Fig. 2. Proposed five-level H-bridge inverter power stage.

The new topology is a single phase configuration that can be used in three phase applications here an open delta primary is acceptable.

II. POWER STAGE

A. Circuit Configuration

Fig. 2 shows the complete power circuit used in the five-level inverter. The H-bridge is formed by the four main power devices, Disp1 to Disp4. A capacitor voltage divider, formed by C1 and
C2 provides a half supply voltage point, node A in Fig. 2. The auxiliary switch, formed by the controlled switch Disp5 and the four diodes, D5 to D8, connects the center point of the left hand half-bridge to node A.

B. Stage Advantages

To probe the reduction in component numbers achieved by this new configuration, Table I

presents the number of components required to implement a five-level inverter using the new topology and three previously defined ones: the two that can be considered as the standard multilevel stages, the diode clamped and the capacitor clamped configurations, and a new and highly improved multilevel stage, the asymmetric cascade configuration [1].

Moreover, the voltage stress and average current in the switches from each topology were calculated in order to compare the power managed by the power switches in each configuration. A resistive load and the same output waveform were considered in all the cases. In order to compare the results, the voltage and current magnitude in the power switches were normalized to the maximum voltage and current in the converter output. This allows to compare different topologies with different dc bus voltages. The results were as follows.

1) Main power switches:

The new topology achieves a 37.5% reduction in the number of main power switches required, using only five controlled power switches instead of the eight required in any of the other three configurations. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches.

2) Auxiliary devices (diodes and capacitors):

—The new configuration reduces the number of diodes by 60% (eight instead of 20) and the number of capacitors by 50% (two instead of four) when compared with the diode clamped configuration.

—The new configuration reduces the number of capacitors by 80% (two instead of 10) when compared with the capacitor clamped configuration.

—The new configuration uses no more diodes or capacitors that the second best topology in the table, the asymmetric cascade configuration.

Additionally, since the two capacitors are onnected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a

TABLE I
COMPARISON BETWEEN FOUR DIFFERENT FIVE-LEVEL INVERTERS TOPOLOGIES

Multilevel inverter type		H bridge, Auxiliary switch	Diode Clamped	Capacitor Clamped	Asymmetric Cascade
Main controlled switches	Number of devices	4	8	8	8
	V_s / V_{oM}	1	0.5	0.5	1
	I_{sM} / I_{oM}	1	1	1	1
	$I_{s(AV)}$ / I_{oM}	0.31	0.31	0.31	0.31
Auxiliary controlled switches	Number of devices	1	0	0	0
	V_s / V_{oM}	0.5	-	-	-
	I_{sM} / I_{oM}	0.5	-	-	-
	$I_{s(AV)}$ / I_{oM}	0.14	-	-	-
Diodes	Number of devices	8	20	8	8
Capacitors	Number of devices	2	4	10	2

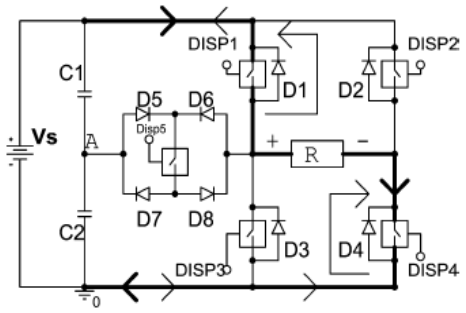


Fig. 3. Switching combination required to generate output voltage level V_S.

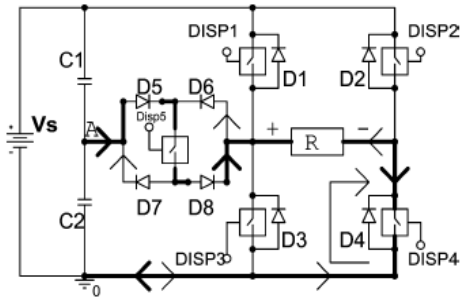


Fig. 4. Switching combination required to generate output voltage level $V_S/2$.

problem that can limit operating range in some other multilevel configurations.

C. Power Stage Operation

The required five voltage output levels(Vs,VS/2,0,-Vs/2,-Vs) are generated as follows:

1) Maximum positive output,Vs : Disp1 is ON, connecting the load positive terminal to Vs , and Disp4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load erminals is Vs . Fig. 3 shows the current paths that are active at this stage.

2) Half-level positive output, Vs/2: The auxiliary switch, Disp5 is ON, connecting the load positive terminal to point A, through diodes D5 and D8, and Disp4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vs/2. Fig. 4 shows the current paths that are active at this stage.

3) Zero output: The two main switches Disp3 and Disp4 are ON, short-circuiting the load. All other controlled switches are OFF; the voltage applied to the load terminals is zero. Fig. 5 shows the current paths that are active at this stage.

4) Half-level negative output, -Vs/2: The auxiliary switch, Disp5 is ON, connecting the load positive terminal to point A, through diodes D6 and D7, and Disp2 is ON, connecting the load negative terminal to . All other controlled switches are OFF; the voltage applied to the load terminals is Vs/2. Fig. 6 shows the current paths that are active at this stage.

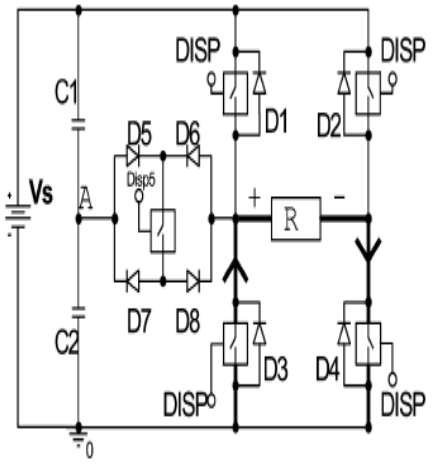


Fig. 5. Switching combination required to generate output voltage level zero.

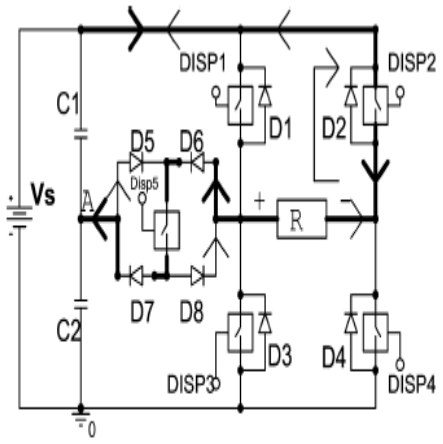


Fig. 6. Switching combination required to generate output voltage level $-V_S/2$.

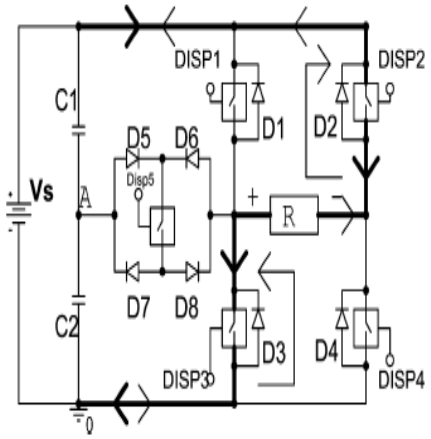


Fig. 7. Switching combination required to generate output voltage level $-V_S$.

5) Maximum negative output: Disp2 is ON, connecting the load negative terminal to Vs, and Disp3 is ON, connecting the load positive erminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is -Vs. Fig. 7 shows the current paths that are active at this stage.

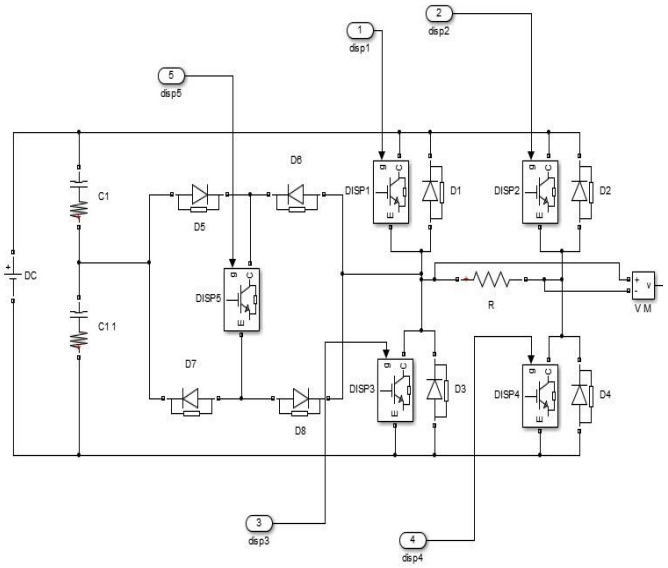
Table II lists the switching combinations that generate the required five output levels (Vs,VS/2,0,-Vs/2,-Vs) .

In this configuration the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

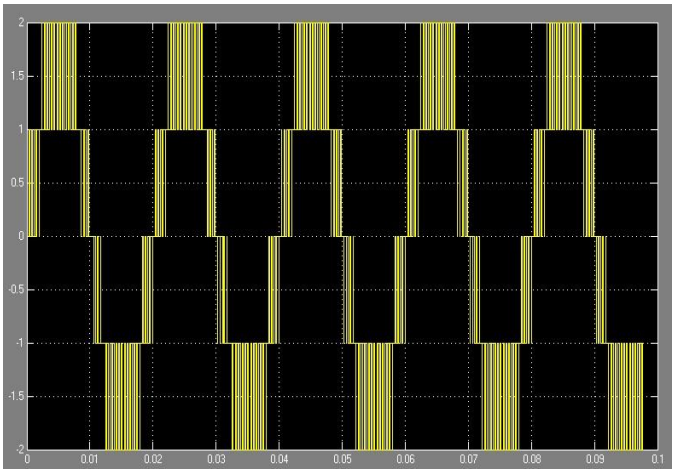
TABLE II
SWITCHING COMBINATIONS REQUIRED TO GENERATE THE FIVE-LEVEL OUTPUT VOLTAGE WAVEFORM

Disp1	Dips2	Disp3	Disp4	Disp5	V_{RL}
on	off	off	on	off	V_S
off	off	off	on	on	$V_S/2$
off	off	on	on	off	0
off	on	off	off	on	$-V_S/2$
on	off	off	on	off	$-V_S$

III. DIAGRAM AND SIMULATION RESULTS



SIMULATION DIAGRAM OF THE SYSTEM



SIMULATION OUTPUT FOR 5 LEVEL

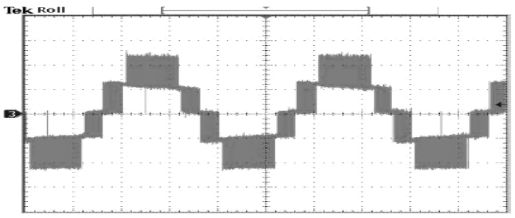


Fig. 19. Output voltage measured on the RL load. Modulation frequency: 10 kHz; modulation index: 0.8 (Vert.: 50 V/div, Horiz.: 4 ms/div).

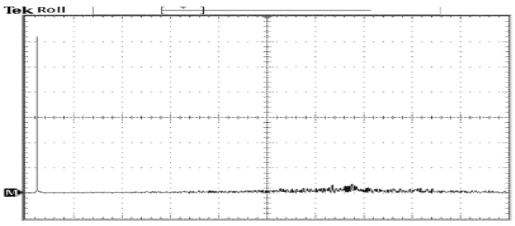


Fig. 20. Five-level converter output voltage frequency spectrum calculated by the Tektronix scope. Output voltage measured on the RL load. Modulation frequency: 10 kHz; modulation index: 0.8 Upper frequency 2.5 kHz. (Vert.: 20 V/div, Horiz.: 250 Hz/div.).

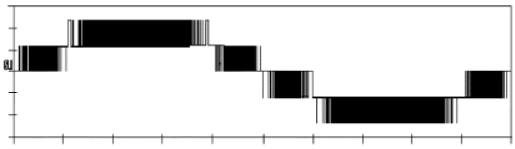


Fig. 15. Simulated five-level converter output voltage. (V_{DC} bus: 120 V; adaptive modulator sample frequency: 200 kHz; modulation index: 0.8; Load: $R = 50\ \Omega$, $L = 3$ mH, $C = 50\ \mu$ F), (Vert.: 50 V/div. Horiz.: 2 ms/div).

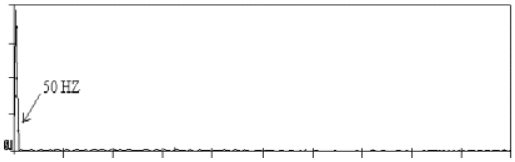


Fig. 16. Five-level converter output voltage frequency spectrum calculated by ORCAD-PSPICE, 200 kHZ modulator sampling frequency (upper frequency: 10 kHz), (Vert.: 25 V/div, Horiz.: 1 Khz/div).

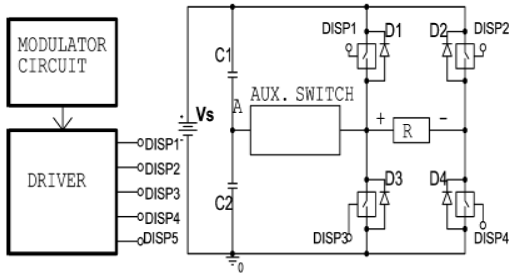
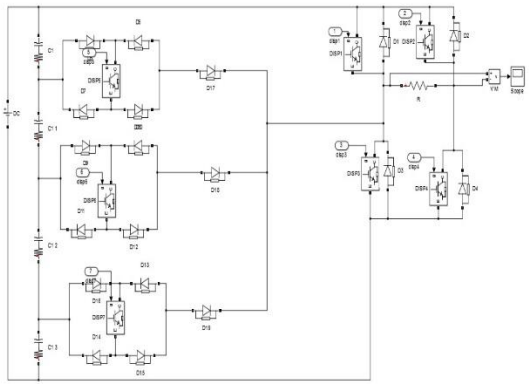


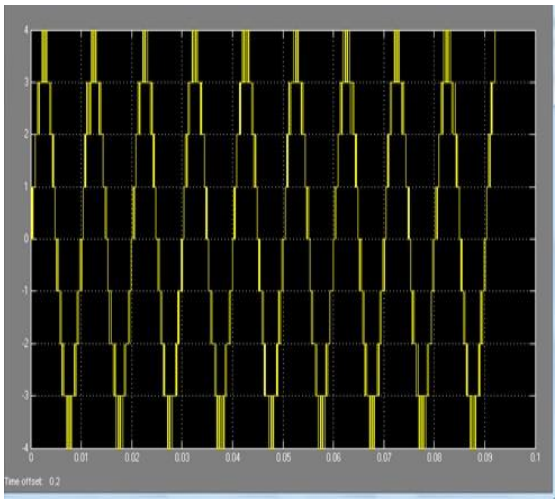
Fig. 17. Experimental validation circuit block diagram.

IV.FUTURE WORK

We trying to modify this above model to get the 9 level output. The simulation diagram and expected output given bellow.



Simulation diagram for 9 level inverter



Expected output

V. CONCLUSION

The agreement between the simulated results and the data taken from the experimental circuit show clearly that:

—the new multilevel topology with the bidirectional auxiliary switch works as expected, generating the required five-level output using only five power switches, and only one center tap provided by two capacitors;

—this topology can be operated at very high modulation frequencies (operation at 200 KHz has been presented), producing a very clean output spectrum;

—this configuration reduced circuit complexity will be adequate for low-medium power applications where standard multilevel inverters can not compete with two-level configurations due to cost, such as low-medium power UPS systems;

—the modulator circuit implemented using a FPGAIC is able to generate all the control signals required to operate the five-level converter, controlling both the commutation sequences and the output amplitude by pulse width modulation. The combined use of these two technologies may lead to the design of multilevel converters at a cost competitive with that of standard two-level converters. A further development of the proposed topology, able to be applied to any number of voltage levels within the power switches maximum voltage, is now under consideration. As shown in Fig. 25, the converter power stage under study will consist of an H-Bridge, bidirectional auxiliary switches, and an -level capacitor voltage divider.

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